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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,713	08/25/2003	Paschal T. Minogue	T0461.70042 US00	5360

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EXAMINER	
JEAN PIERRE, PEGUY	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,713	MINOGUE, PASCHAL T.	
	Examiner	Art Unit	
	Peguy JeanPierre	2819	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-6, and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Lipasti et al. (USP 6,600,789).

With regard to claims 1 and 4, Lipasti et al disclose in Figure 1 an analog to digital converter that receives an analog input signal and generates a multi bit (m) digital signal. The m-bit digital signal is converted to a single bit (n) digital signal. With regard to claims 2 and 6, the multi bit digital signal is generated from a sigma delta modulator (2), with regard to claims 3, 5, and 6 the conversion of the m-bit to an n-bit converter a noise shaping digital sigma delta modulator (3); with further regard to claim 1 and claim 5, the noise shaping converter comprises a quantizer (408) which quantizes the m-bit digital signal to a single bit digital signal. It is inherent that the single bit digital signal can be applied/outputted to any interface (bus) device that process digital data.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 18, 20 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Melanson (USP 6,340,940).

With regard to claims 18 and 20, Melanson discloses in Figure 4 a digital to analog converter that converts s= 1-bit digital data to t=multi-bit digital data. The system comprises a digital to analog converter that converts the multi-bit digital data to analog output. It is inherent that any digital interface (bus) device can be made to output a single bit digital data for further processing.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-9 and 11-15, 21-23, 25-32, 35-38, 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipasti et al. (USP 6,600,789) in view of Melanson (USP 6,340,940).

With regard to claims 7 and 13-15, Lipasti et al. disclose essential features of the claimed invention. Lipasti et al. further disclose means to decimate or interpolate single or multi-bit digital data (see col. 1, lines 21-28). However, Lipasti et al. fail to teach a processing means that is arranged to receive the n=1-bit digital signal and to generate an output digital signal. Melanson discloses a digital to analog converter that is

considered as a processing device. The system of Melanson receives a single bit digital data that inherently being supplied from another digital device. Such digital device to be operative must be connected to the processing of Melanson by an interface. With regard to claims 21-23 and 25-29, the systems of Melanson et al. (second section) can be connected at its front end by the system of Lipasti et al. (first section). Both systems can be wired, or be bussed or made to interface with each other to facilitate transfer of bit from one system to another. With regard to claims 35, 38, 41-44 the conversion of analog to digital, the conversion form digital to digital and the transfer of bit from system to another is as follow: Lipasti et al. converts analog input signal to a multi-bit data (m) that is quantized (408) to generate a 1-bit (n) digital output (5) (m>n). The one-bit output is inputted into the system of Melanson through a bus or interface ((Fig. 1 102) to be further processed through a modulator (202) (m=p) and a DEM (203) that converts the 1-bit signal to multi-bit (n<p) and outputs an analog signal via a low pass filter (204) coupled to the output of the multi-bit DAC (203). Melanson processor receives a single bit input that can be provided by the system of Lipasti et al. since the output of Lipasti et al. is single bit digital signal. Lipasti et al. converts a multibit to a single bit, and Melanson converts the single bit (from Lipasti et al.) to a multi-bit. (Note that any letter can be used to designate the bit conversion process (m, n, s, t, r, p etc...). Any artisan having working knowledge in the art would have been motivated to combine the teachings of Lipasti et al. and Melanson by supplying the single bit output of the modulator of Lipasti et. al to the input of the processor of Melanson for the benefit of laying out both conversion formats on the same or different integrated chip as desired.

With regard to claims 8, 9, 12, 30-33, 36-37, the n=1 bit data received by Melanson from the system of Lipasti et al. is converted to p=multi-bit data through a sigma delta modulator that has a low pass characteristic (see col.3, lines 63-66 and col. 4, lines 1-5) that filters out the digital signal.

7. Claims 4 10, 19, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipasti et al. (USP 6,600,789) and Melanson (USP 6,340,940) further in view of Desrosiers et al. (USP 6,140,946).

With regard to claims 4, 10, 19, and 24 of converting a 1-bit to multi-bit at a substantially the same rate, Lipasti et al. and Melanson do not teach the above limitations. Desrosiers et al. disclose a method of converting multibit data (parallel) to single bit data (serial) with a clock frequency having the ratio of 1. That is the conversion is done at substantially the same rate. Therefore, any artisan having working knowledge in the art presented with the teaching of Desrosiers et al. would have motivated to modify the system of Melanson and Lipasti et al. by clocking the input and the output of the system at substantially the same rate to increase the speed of the converter.

8. Claims 16-17 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipasti et al. (USP 6,600,789) and Melanson (USP 6,340,940) further in view of Tang et al. (USP 5,103,274).

With regard to claims 16-17 and 33-34 of providing the first and the second section with different manufacturing geometry, Lipasti et al. and Melanson do not teach the above limitations. Tang et al. teach the use of different manufacturing geometry in designing/fabricating floating gate memory devices. The system of Tang et al. uses both

coarser (double polycrystalline structure) and finer (single polycrystalline structure) manufacturing geometry to reduce the size of the MOS gates. Therefore, any artisan having working knowledge in the art presented with the teaching of Tang et al. would have been motivated to use the manufacturing geometry as taught by Tang et al. to minimize the size, reduce memory cell size so critical in electronic devices.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Raghavan et al (USP 6,441,759), Yamaguchi (USP 6,404,368), Reefman (USP 6,606,043), Nestler (USP 6,307,493), Fujimori (USP 6,326,912), Linz (USP 6,005,505) disclose sigma delta modulator analog/digital converter.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peguy JeanPierre whose telephone number is (571) 272-1803. The examiner fax phone number is (571) 273-1803.

Peguy JeanPierre
Primary Examiner